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JAN 25 2002



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Docket No.: M-7469 US

January 25, 2002

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BOX NON-FEE AMENDMENT
Commissioner for Patents
Washington, D.C. 20231

Re: Applicants: Yuesong He; Ken Kuohua Chang; R. Lee Tan
Assignee: Advanced Micro Devices, Inc.
Title: Method And Apparatus For Improved Performance Of Flash Memory Cell Devices
Serial No.: 09/492,243
Examiner: E. Ortiz
Docket No.: M-7469 US Filed: January 27, 2000
Group Art Unit: 2815

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

- (1) Return Receipt Postcard;
- (2) This Transmittal Letter (in duplicate); and
- (3) Response to Office Action (10 pages).

No additional fee is required.
 The fee has been calculated as shown below:

CLAIMS AS AMENDED

	Claims Remaining <u>After Amendment</u>		Highest No. Previously Paid For		Present Extra	Rate		Additional Fee
Total Claims	6	Minus	20	=	0	x \$18.00	\$	0.00
Independent Claims	2	Minus	3	=	0	x \$84.00	\$	0.00
	<input type="checkbox"/> Fee of _____ for the first filing of one or more multiple dependent claims per application						\$	
	<input type="checkbox"/> Fee for Request for Extension of Time						\$	

Total additional fee for this Amendment: \$ 0.00

Conditional Petition for Extension of Time: If an extension of time is required for timely filing of the enclosed document(s) after all papers filed with this transmittal have been considered, an extension of time is hereby requested.

Please charge our Deposit Account No. 19-2386 in the amount of \$ 0.00

Also, charge any additional fees required and credit any overpayment to our Deposit Account No. 19-2386.

Total: \$ 0.00

EXPRESS MAIL LABEL NO.:
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Respectfully submitted,

Jon W. Hallman
Attorney for Applicants
Reg. No. 42,622

U.S. PATENT AND TRADEMARK OFFICE
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Yuesong He; Ken Kuohua Chang; R. Lee Tan #7/9
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Newport Beach, California
January 25, 2002

Box Non-Fee Amendment
COMMISSIONER FOR PATENTS
Washington, D.C. 20231

RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action dated October 25, 2001, please amend the above-identified application as follows.

IN THE CLAIMS

Please amend Claim 3 and 9 as follows:

M&B D
G'

3. (amended) A memory array comprising a plurality of floating gate transistors connected in series, each floating gate transistor having formed, in a well of a substrate, a source and a drain region and a channel region separating said source and drain regions, said channel region having a non-uniform concentration of dopant; wherein said non-uniform concentration comprises a retrograde concentration distribution in the direction from the surface of the substrate, and wherein said non-uniform concentration comprises a lateral concentration distribution along the length of the channel that is higher in a region generally

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